

Figures 1-3 of the Drawings are objected to as not being labeled "Prior Art."

Claims 1-6, 9, 10, 12-22, 24, 25 and 27-30 stand rejected under 35 U.S.C. § 102 (b) as being considered to be anticipated by U.S. Patent No. 5,661,663 to Scepanovic et al. ("Scepanovic") and also stand rejected under 35 U.S.C. § 102(e) as being considered to be anticipated by U.S. Patent No. 6,260,177 to Lee et al. ("Lee").

Claims 7-8, 11, 23 and 26 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Figures 1-3 of the Drawings stand objected to because they are not labeled as "Prior Art" as is alleged to be indicated in the brief description of the drawings.

Applicants respectfully request that the Drawings be amended as indicated in the proposed Figures 1-3 submitted concurrently herewith to address the above objections. More particularly, Figures 1-3 have been amended to include the legend "Prior Art."

Accompanying this Amendment is (1) a separate document entitled "Request to Approve Drawing Changes" and (2) sketches prepared in accordance with 37 C.F.R. § 1.123 showing the proposed changes in red ink.

Claims 1-6, 9-10, 12-22, 24-25 and 27-30 stand rejected under 35 U.S.C. 102(b) as being considered to be anticipated by Scepanovic.

Claim 1 includes the limitations

identifying partial feasible routing solutions corresponding to  
each of a subset of a set of wires to be routed;  
merging the partial feasible routing solutions to identify one  
or more feasible routing solutions for the set of wires to be routed.

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(Claim 1)(emphasis added).

Applicants respectfully submit that Scepanovic does not teach the claimed features of applicants' invention including at least identifying partial feasible routing solutions and merging the partial feasible routing solutions to identify one or more feasible routing solutions for a set of wires to be routed.

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Scepanovic discloses a method of producing a placement of cells for an integrated circuit. The approach disclosed in Scepanovic includes constructing a hierarchical cluster tree in which a lowest level of the tree includes clusters of interconnected cells and each successively higher level includes clusters of interconnected clusters from a successively lower level. Clusters in each level are merged by a min-cut operation (Scepanovic, Abstract.)

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In accordance with Scepanovic, each cell represents a single logic element such as a gate or several logic elements that are interconnected in a standardized manner to perform a specific function. Thus, the approach of Scepanovic is primarily concerned with placement of cells in a layout.

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In contrast, claim 1 sets forth an approach for routing interconnects between cells that have already been placed. In particular, claim 1 sets forth an approach including identifying multiple feasible routing solutions for a wire to be routed. In this context, a wire to be routed is to be routed between two fixed points and the multiple feasible routing solutions comprise the variety of ways the wire can be routed between those two fixed points.

While Scepanovic discloses interconnections between cells, these interconnections merely indicate which cells are connected together and not the particular route for the interconnection. More specifically, Scepanovic does not disclose identifying multiple feasible routing solutions, i.e. multiple different paths

5 that can be used to create a given connection between two defined points.

Where Scepanovic discusses different ways of interconnecting cells, the different approaches merely relate to changes in cell placement and/or different orders in which to chain together a group of cells and not to a variety of ways to route a wire between two given points. (See e.g. Scepanovic, col. 6, line 41 – col. 7, line

10 20.

For at least the foregoing reasons, Scepanovic does not teach identifying partial feasible routing solutions or merging partial feasible routing solutions as set forth in claim 1. Nor does Scepanovic suggest such features. There is no indication in Scepanovic of identifying more than one route for a wire between

15 two given points.

Independent claims 9, 15, 20, 22 and 27 each include limitations similar to those argued above in reference to claim 1. Claims 2-8, claims 10-14, claims 16-19, claim 21, claims 23-26 and claims 28-30 depend from and further limit claims 1, 9, 15, 20, 22 and 27, respectively, and thus, should also be found

20 allowable for at least the same reasons.

Claims 1-6, 9-10, 12-22, 24-25 and 27-30 further stand rejected under 35 U.S.C. 102(e) as being considered to be anticipated by Lee.

Applicants respectfully submit that Lee also does not teach or suggest the claimed features of Applicants' invention.

Lee discloses the automatic configuration of gate array cells using a standard cell function library. In accordance with Lee, a standard cell netlist at 5 the transistor level is compiled to list the transistors required in implementing the desired functions. Based on the netlist, gate array cells are restructured so that they can be inserted in desired locations designed for standard cells. The restructured gate array cells which are made up of single poly and double poly structures are placed in the layout and then connected using the function net 10 connectivity patterns from the standard cell function library. (Lee, Abstract).

In accordance with one aspect of Lee, PMOS and NMOS structures are assigned to single poly structures and then two single poly structures are merged to form a double poly structure. It is asserted in the Office Action that this aspect of Lee teaches the multiple feasible routing solutions. Applicants respectfully 15 assert that such a characterization is improper. These steps shown in Figure 7 relate to configuring a gate array cell and not to routing wires.

There is no disclosure in Lee of identifying multiple feasible routing solutions for a wire or of merging these feasible routing solutions. There is also no suggestion of such features.

20 For at least the foregoing reasons, claim 1 is patentably distinguished over the Lee reference. Further, due to the similar limitations in the independent claims and the dependencies of the dependent claims, claims 2-30 are also patentably distinguished over the Lee reference.

Applicants respectfully submit that the applicable objections and rejections have been overcome and claims 1-30 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, he is invited to telephone applicants' representative at the number 5 indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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